

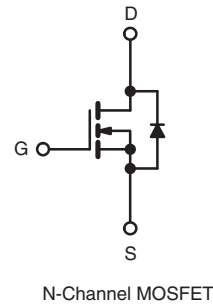
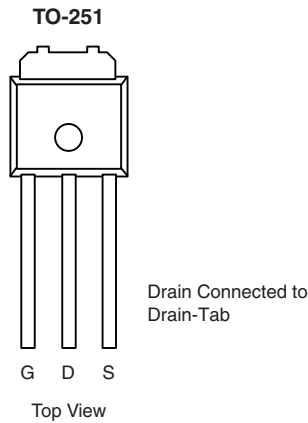
## SW6N70DB-VB TO251 Datasheet

### Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	700	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	1.9
$Q_g$ (Max.) (nC)	130	
$Q_{gs}$ (nC)	17	
$Q_{gd}$ (nC)	72	
Configuration	Single	

#### FEATURES

- Dynamic  $dV/dt$  rating
- Repetitive avalanche rated
- Isolated central mounting hole
- Fast switching
- Ease of paralleling
- Simple drive requirements



ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V <sub>DS</sub>	700	V
Gate-Source Voltage			V <sub>GS</sub>	± 20	
Continuous Drain Current	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	I <sub>D</sub>	6.0	A
		T <sub>C</sub> = 100 °C		4.2	
Pulsed Drain Current <sup>a</sup>			I <sub>DM</sub>	24	
Linear Derating Factor				1.2	W/°C
Single Pulse Avalanche Energy <sup>b</sup>			E <sub>AS</sub>	490	mJ
Repetitive Avalanche Current <sup>a</sup>			I <sub>AR</sub>	5.4	A
Repetitive Avalanche Energy <sup>a</sup>			E <sub>AR</sub>	15	mJ
Maximum Power Dissipation	T <sub>C</sub> = 25 °C		P <sub>D</sub>	150	W
Peak Diode Recovery dV/dt <sup>c</sup>			dV/dt	2.0	V/ns
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Soldering Recommendations (Peak Temperature) <sup>d</sup>	for 10 s			300	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 31\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 5.4\text{ A}$  (see fig. 12).
- $I_{SD} \leq 5.4\text{ A}$ ,  $dI/dt \leq 120\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq 600$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.24	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.83	

**SPECIFICATIONS** ( $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		700	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA		-	0.98	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 700 V, V <sub>GS</sub> = 0 V		-	-	100	μA
		V <sub>DS</sub> = 560 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	500	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 3.2 A <sup>b</sup>	–	1.9	-	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 100 V, I <sub>D</sub> = 3.2 A <sup>b</sup>		3.0	-	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5		-	1900	-	pF
Output Capacitance	C <sub>oss</sub>			-	470	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	280	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 5.4 A, V <sub>DS</sub> = 350 V, see fig. 6 and 13 <sup>b</sup>	-	-	130	nC
Gate-Source Charge	Q <sub>gs</sub>			-	-	17	
Gate-Drain Charge	Q <sub>gd</sub>			-	-	72	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 350 V, I <sub>D</sub> = 5.4 A, R <sub>g</sub> = 9.1 Ω, R <sub>D</sub> = 75 Ω, see fig. 10 <sup>b</sup>		-	16	-	ns
Rise Time	t <sub>r</sub>			-	36	-	
Turn-Off Delay Time	t <sub>d(off)</sub>			-	100	-	
Fall Time	t <sub>f</sub>			-	32	-	
Internal Drain Inductance	L <sub>D</sub>	Between lead, 6 mm (0.25") from package and center of die contact		-	5.0	-	nH
Internal Source Inductance	L <sub>S</sub>			-	13	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		-	-	5.4	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	22	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 5.4 A, V <sub>GS</sub> = 0 V <sup>b</sup>		-	-	1.8	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 5.4 A, dI/dt = 100 A/μs <sup>b</sup>		-	550	830	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	2.4	3.6	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
 b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

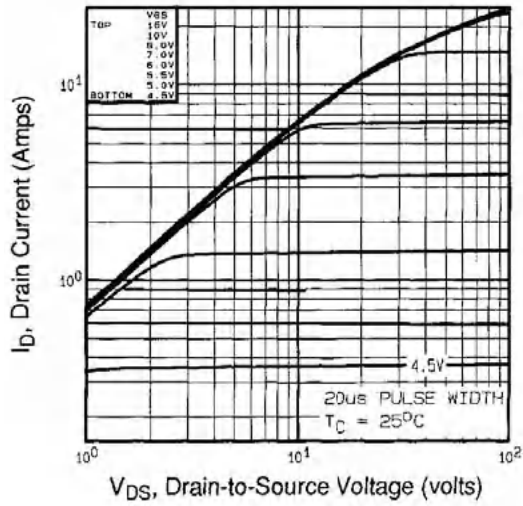


Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^{\circ}\text{C}$

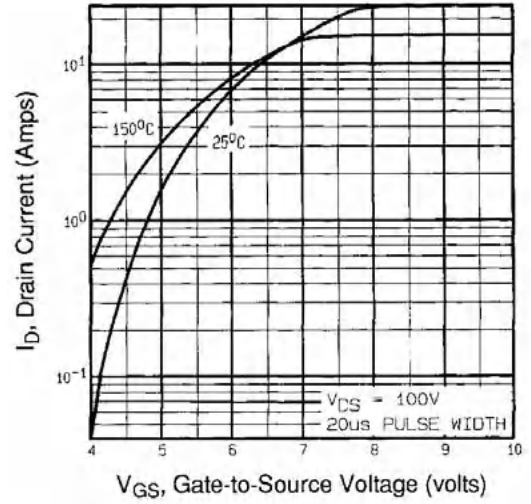


Fig. 3 - Typical Transfer Characteristics

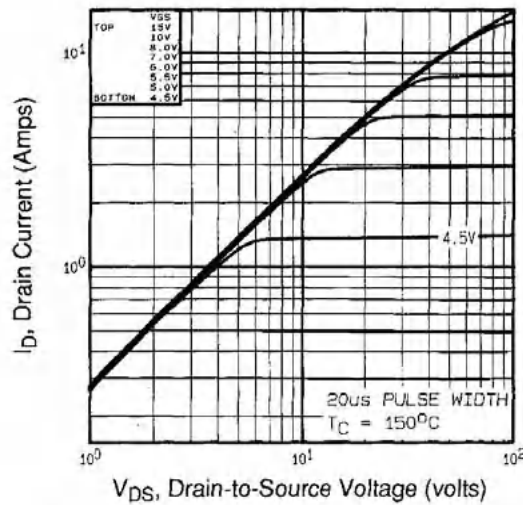


Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^{\circ}\text{C}$

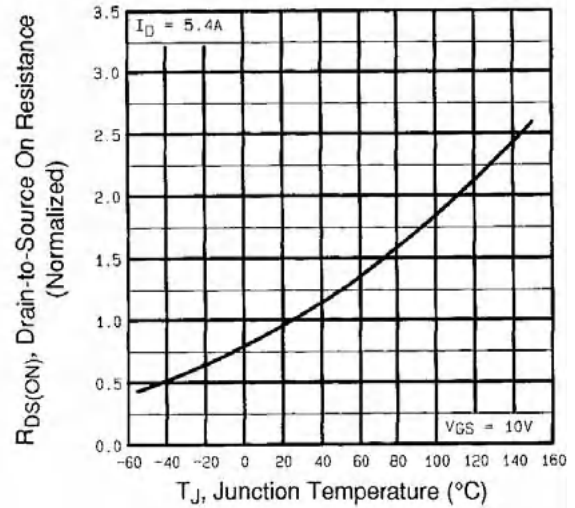


Fig. 4 - Normalized On-Resistance vs. Temperature

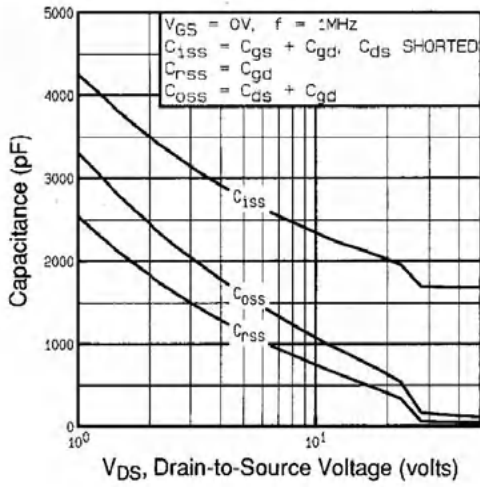


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

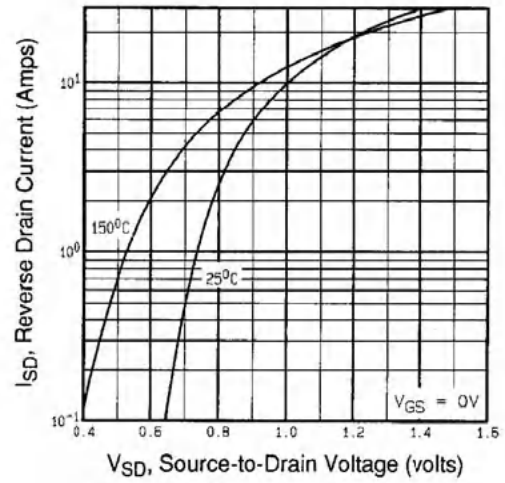


Fig. 7 - Typical Source-Drain Diode Forward Voltage

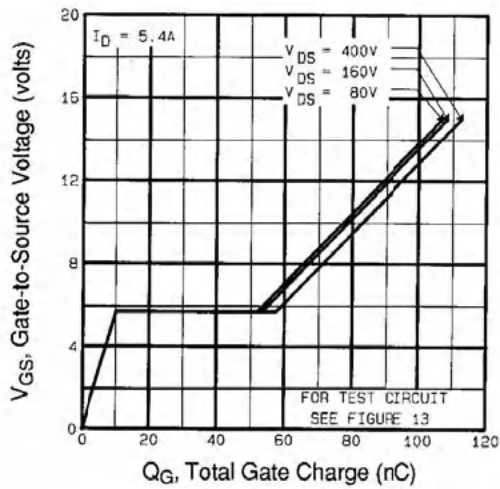


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

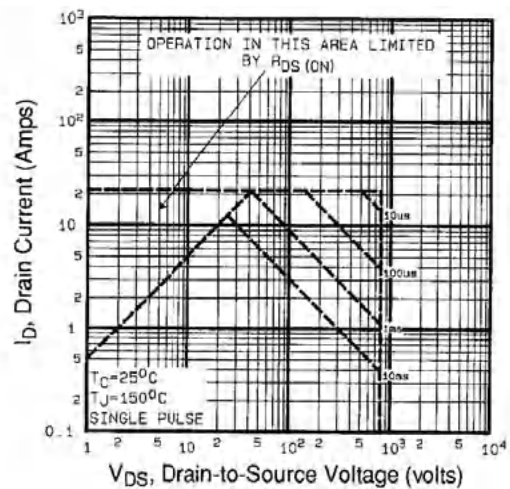


Fig. 8 - Maximum Safe Operating Area

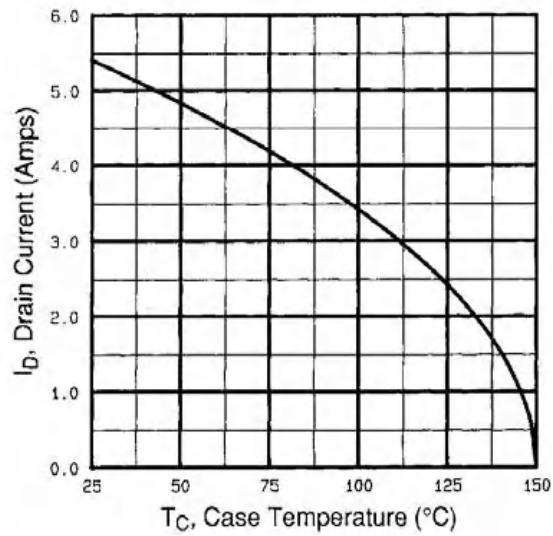


Fig. 9 - Maximum Drain Current vs. Case Temperature

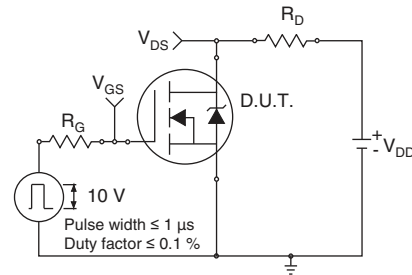


Fig. 10a - Switching Time Test Circuit

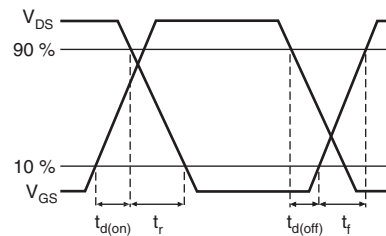


Fig. 10b - Switching Time Waveforms

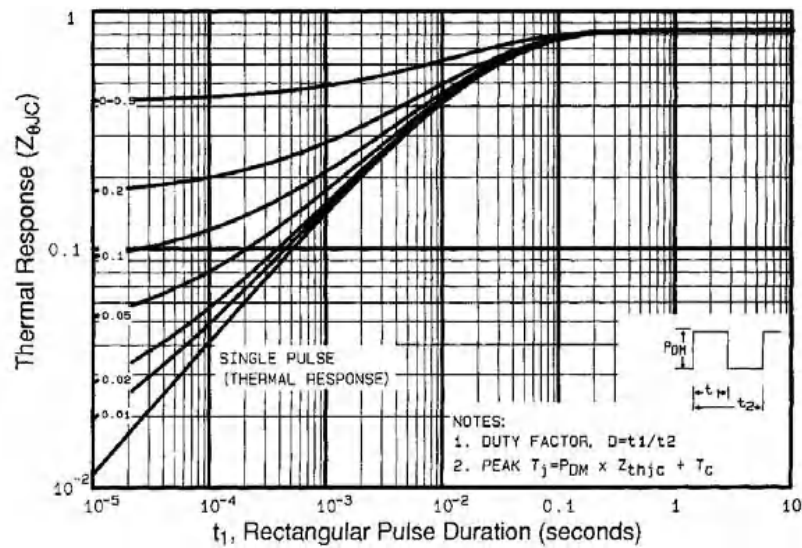


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

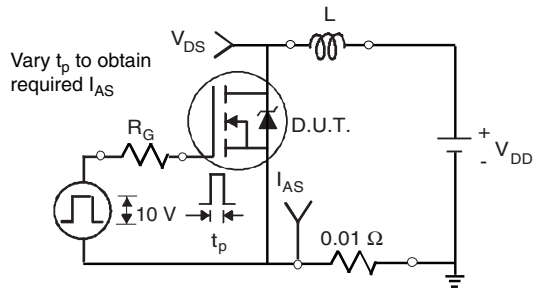


Fig. 12a - Unclamped Inductive Test Circuit

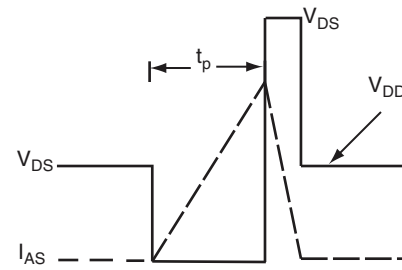


Fig. 12b - Unclamped Inductive Waveforms

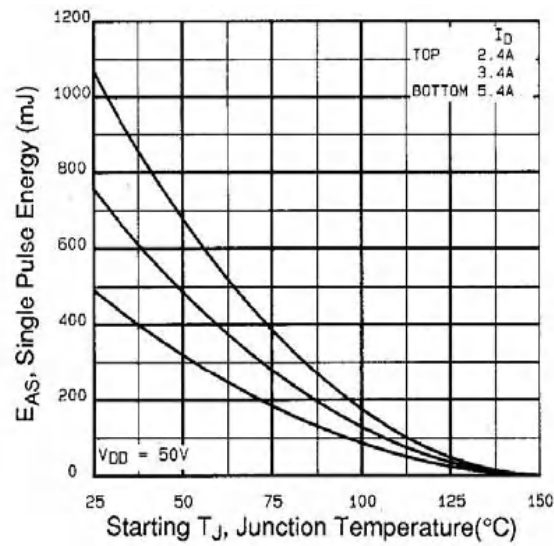


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

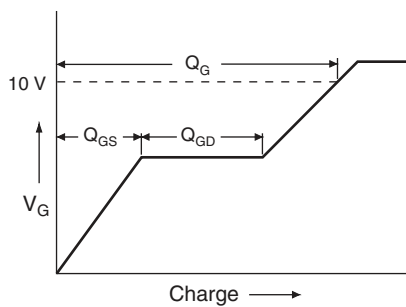


Fig. 13a - Basic Gate Charge Waveform

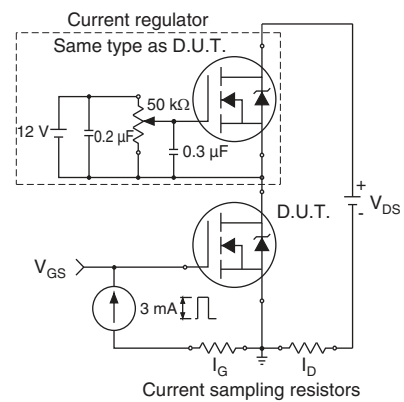
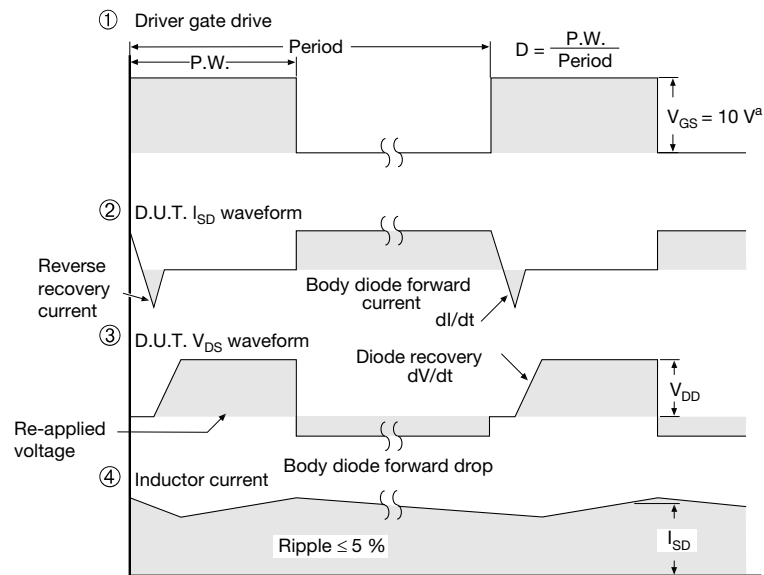
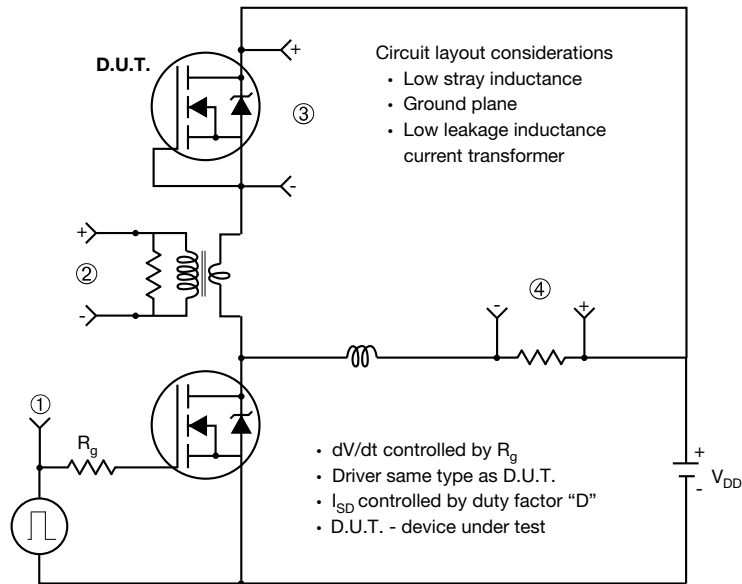


Fig. 13b - Gate Charge Test Circuit

**Peak Diode Recovery dV/dt Test Circuit**

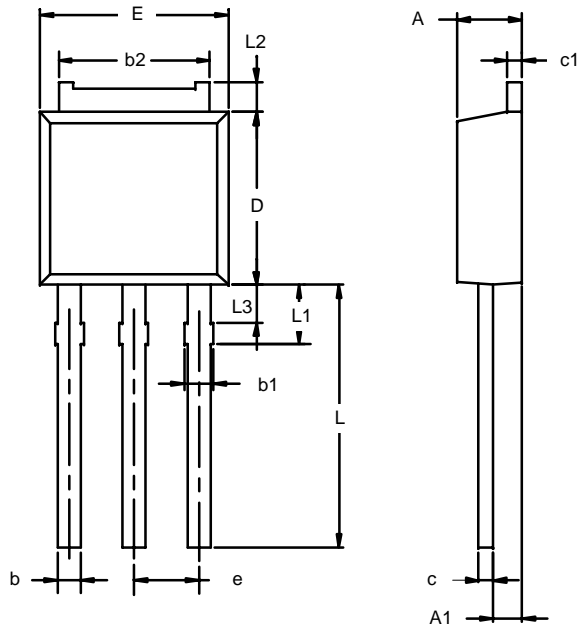


**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**



**TO-251AA (DPAK)**

Note: Dimension L3 is for reference only.

Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
<b>A</b>	2.21	2.38	0.087	0.094
<b>A1</b>	0.89	1.14	0.035	0.045
<b>b</b>	0.71	0.89	0.028	0.035
<b>b1</b>	0.76	1.14	0.030	0.045
<b>b2</b>	5.23	5.43	0.206	0.214
<b>c</b>	0.46	0.58	0.018	0.023
<b>c1</b>	0.46	0.58	0.018	0.023
<b>D</b>	5.97	6.22	0.235	0.245
<b>E</b>	6.48	6.73	0.255	0.265
<b>e</b>	2.28 BSC		0.090 BSC	
<b>L</b>	3.89	9.53	0.153	0.375
<b>L1</b>	1.91	2.28	0.075	0.090
<b>L2</b>	0.89	1.27	0.035	0.050
<b>L3</b>	1.15	1.52	0.045	0.060



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